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Date: November 22, 2005 By: Sherry Duncan Bitler
Sherry Duncan Bitler

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	John Erik LINDHOLM, et al.	Confirmation No.:	7963
Serial No.	10/032,894	Examiner:	J. C. WANG
Filed:	10/26/2001	Art Unit:	2672

FOR: LIGHTING SYSTEM AND METHOD FOR A GRAPHICS PROCESSOR

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TRANSMITTAL

Enclosed are the following documents:

[x] 37 C.F.R. § 1.193 Supplemental Reply Brief (in triplicate); and
[x] Return receipt postcard

[] A check for the total fee is attached.

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The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§1.16, 1.17, and 1.21 that may be required by this paper, and to credit any overpayment, to Deposit Account No. 03/3117.

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37 C.F.R. § 1.193 SUPPLEMENTAL REPLY BRIEF

Sir:

Applicants submit that the Examiner has still not established proper grounds for rejecting claims 24-25 and 27-34. In particular, the Examiner still fails to point to elements in *Krech* (U.S. Patent No. 6,184,902) that correspond to applicants' claim elements. For example, the Examiner fails to point to an element in *Krech* that properly corresponds to applicants' claimed "lighting logic unit." Additionally, the Examiner does not properly identify the conversion module nor address the coupling between the lighting logic unit, the multiplication logic, and the conversion module. And further, the Examiner fails to point to an element in *Krech* that corresponds to applicants' claimed multiplication logic that includes a feedback loop. These issues are addressed below under the corresponding headings. Although Applicants focus only on a subset of the arguments set forth in the Appeal Brief and Reply Brief, Applicants are not waiving any of

those previously presented arguments by focusing on a subset of those arguments in this Supplemental Reply Brief.

I. OVERVIEW OF THE EXAMINER'S POSITION

Before addressing the merits of the Examiner's positions, a brief overview of those positions may be helpful. Claims 24, 30, and 34 recite a few basic elements: an input buffer, a multiplication logic unit, an arithmetic logic unit, a register unit, and a lighting logic unit. These elements are described specifically in the claims and this overview is not meant to replace that claim language. Rather, this overview is meant to provide a starting point for understanding the Examiner's positions.

In the Answer, Supplemental Answer and the previous Office Actions, the Examiner identified the *Krech* elements that supposedly corresponded to applicants' claimed elements. As shown from the table below, at times the Office Actions did not designate with any particularity those portions of the prior art that allegedly correspond to the claim limitations. Moreover, the Examiner's position has changed with every paper received from the Examiner; nonetheless, applicants believe that the chart below accurately sets forth the Examiner's positions.

Element Recited In Applicant's Claim	**Examiner's May 5, 2004 (Final Office Action) Position Regarding The Corresponding Element in *Krech***	**Examiner's July 12, 2004 (Advisory Action) Position Regarding The Corresponding Element in *Krech***	**Examiner's January 27, 2005 Position Regarding The Corresponding Element in *Krech***	**Examiner's September 22, 2005 Position Regarding The Corresponding Element in *Krech***
input buffer	Figures 2-3	Figure 5	input buffer 77 (Figure 5)	input buffer 77 (Figure 5)
multiplication logic unit	Fig. 3--element 55.	Not Addressed	multiplier 55 (Figure 5)	multiplier 55 (Figure 5)
Arithmetic logic unit	Col. 3, lines 22-34.	Not Addressed	ALU 54 (Figure 5)	ALU 54 (Figure 5)
register unit	Col. 14, lines 28-55	Not Addressed	registers 61 (Figure 5)	registers 61 (Figure 5)
lighting logic unit	Col. 3, lines 22-34; figs 3-5	Figure 5	control unit logic element 115 (Figure 5)	Branch central intelligence 112, state management address decode 132, vertex/light counter 139 or a control logic element 115
conversion module	Particular part of *Krech* relied on not designated—mere reference to Figure 5	Figure 5	Control unit 17	Control unit 17
multiplication logic unit with the feedback loop	Particular part of *Krech* relied on not designated; instead office action merely references Col. 11, line 45 Col. 13, line 15; fig 7.	Particular part of *Krech* relied on not designated; instead office action merely references Col. 11, line 45 Col. 13, line 15; fig 7.	Col. 11, line 45 Col. 13, line 15; figs. 5 and 7. A plurality of lines including line 131, line 148, line 151, line 154, line 108 and line 125. Figures 7a and 7b. Column 9.	A plurality of lines including line 131, line 148, line 151, line 154, line 108 and line 125. Col. 11, line 45 Col. 13, line 15; figs. 5 and 7. Column 9.

Table 1: Summary Of The Examiner's Position

Because *Krech* Figure 5 is the core of the Examiner's rejection, it is reproduced below for convenience.

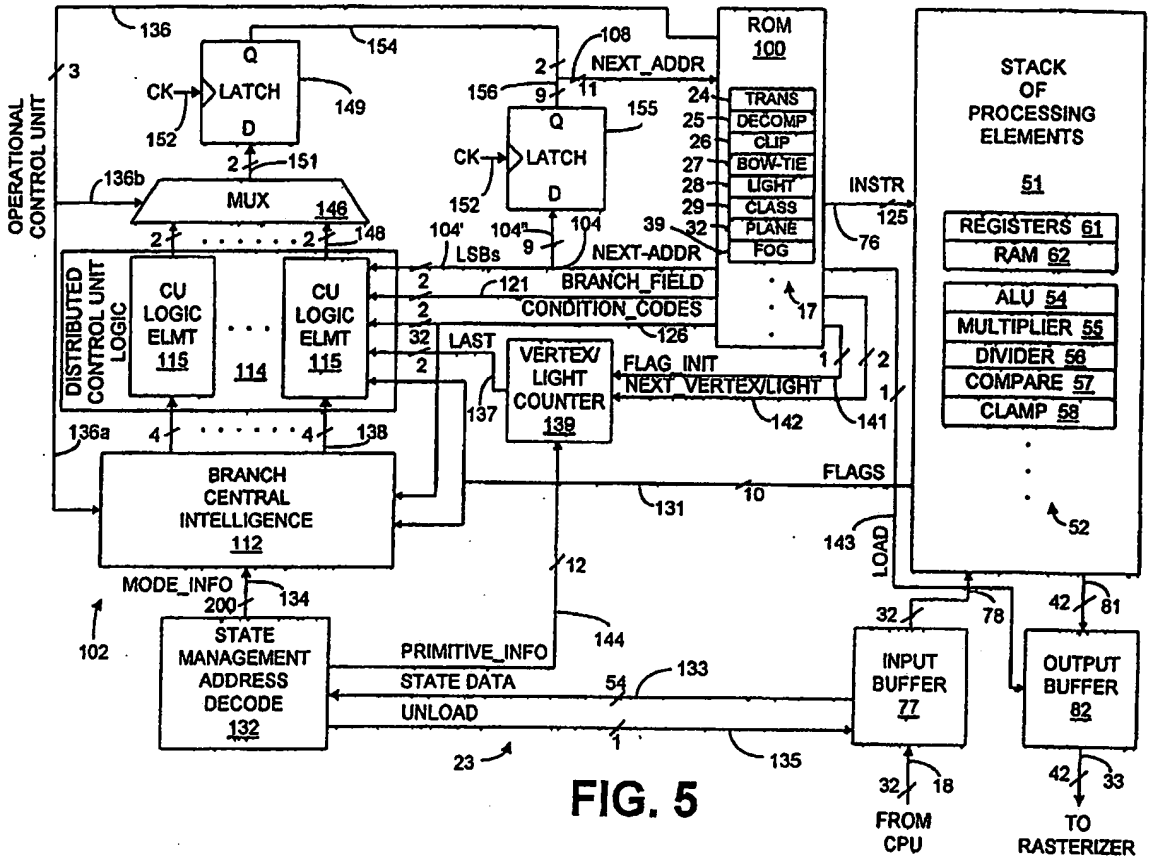

FIG. 5

Krech Figure 5

II. *KRECH* DOES NOT TEACH APPLICANTS' "CLAIMED LIGHTING LOGIC UNIT."

Claim 24 recites "a lighting logic unit coupled to the arithmetic logic unit, the at least one input buffer, and the multiplication logic unit." Notice that the language recites a "lighting logic unit" and a specific relationship between the "lighting logic unit" and the other elements. Claims 30 and 34 recite a similar—although not identical—limitation.

The Examiner now argues that any one of the *Krech* branch central intelligence 112, state management address decode 132, vertex/light counter 139 or a control logic element 115 corresponds to applicants "lighting logic unit" on the basis that each of these elements "carries

lighting logic and therefore meets the limitation of a light logic unit" (See Supplemental Examiner's Answer, page 17, last paragraph). This position is simply untenable because, among other reasons, for example, even a mere conductor (e.g., a wire) carrying lighting logic would disclose a lighting logic unit according to the position of the Examiner.

Although both general lighting modules and elements that carry lighting logic are known in the art, Applicants' claimed lighting logic unit (embodiments of which are described in the specification), and its relationship to the other claimed components, however, is not known in the art.

III. *KRECH* DOES NOT TEACH THAT "THE LIGHTING LOGIC UNIT IS COUPLED TO THE MULTIPLICATION LOGIC UNIT VIA A CONVERSION MODULE."

As described in Section II, *Krech* does not teach applicants' claimed lighting module. Moreover, *Krech* does not disclose applicants' claimed connection of a conversion module of the lighting logic unit and the multiplication logic unit. No element in *Krech* serves as a lighting logic unit and is coupled to the multiplication logic unit via a conversion module.

Moreover, the Examiner has still not identified, and Applicants are unable to find, any construct properly corresponding to Applicant's "conversion module." Instead, the Examiner contends *Krech's* transform mechanism 24, which performs "scaling or moving a vertex in space" corresponds to the "conversion module" recite in claim 1. Applicants' conversion module, however, is "adapted for converting scalar vertex data to vector vertex data." Applicants submit that the Examiner has simply not identified the recited "conversion module" in *Krech.*

In particular, instead of identifying any particular portion of *Krech* that teaches "a conversion module adapted for converting scalar vertex data to vector vertex data" the Examiner first contends that the claim language is "misleading," then appears to ignore the recited claim

language while guessing at what the claim may mean. (See Supplemental Examiner's Answer, page 9, last paragraph). Applicants disagree and submit the claim language is not misleading and that those of skill in the art will understand these are known terms. Although Applicants disagree with the Examiner, Applicants submit that the merits of the Examiner's statements are irrelevant because the Examiner simply has not identified a conversion module adapted for "converting scalar vertex data to vector vertex data." As a consequence, the rejection against claim 24 can not properly stand.

IV. *KRECH* DOES NOT TEACH APPLICANTS' CLAIMED MULTIPLICATION LOGIC UNIT WITH A FEEDBACK LOOP.

Claim 30 recites that the "multiplication logic unit has a feedback loop coupled to an input of the multiplication logic unit." The Examiner contends that the recited "feedback loop" corresponds to a plurality of lines including line 131, line 148, line 151, line 154, line 108 and line 125. Applicants stand by their previous arguments that the material that the Examiner cites as teaching a feedback loop has no relation to the *Krech* multiplier 55 or to any other multiplication logic unit.

Moreover, even assuming that the identified collection of lines, beginning with line 131, and ending with instruction line 125 form some part of a feedback loop, claim 30 recites a multiplication logic unit that has a feedback loop coupled to "an input of the multiplication logic unit." As shown, in Figure 5 of *Krech*, however, the collection of lines beginning with line 131 and ending with instruction line 125 simply does not couple to the input of *Krech's* multiplier 55, and as a consequence, cannot correspond to Applicants "feedback loop" that is coupled to "an input of the multiplication logic unit." Accordingly, the rejection against claims 30 and 34 can not stand.

SUMMARY

Applicants disagree with much of the Examiner's characterization of the state of the art, the references, and applicant's technology. But as is appropriate for a reply brief, applicants only address certain portions of the Examiner's answer.

All of the pending claims are patentable for the reasons set forth herein, and Appellant respectfully requests such finding.

Three copies of this Reply Brief are provided.

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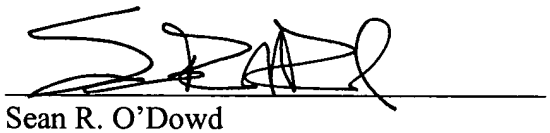
By: 

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